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Claims after this response:

1(Currently Amended). A circuit comprising:

a plurality of processing blocks on a first ~~substrate~~ chip; and

an interconnect network comprising a plurality of network nodes arranged in a two-dimensional array on said first chip ~~substrate~~, each network node having a plurality of adjacent network nodes and being connected to each adjacent network node by a communication bus that connects only those two network nodes and processing blocks adjacent to that bus;

each network node comprising:

a plurality of communication ports, each communication port comprising an input port for receiving digital signals and an output port for transmitting digital signals on a bus connected to that communication port;

a programmable switch that selectively connects one of said input ports to one of said output ports in response to connection information stored in a memory in that network node, wherein;

each processing block is connected to one of said communication buses and sends and/or receives data on that bus, each processing block performing a predetermined processing function, said processing block being located within said two-dimensional array of network nodes.

2(Original). The circuit of Claim 1 wherein said connection information is stored in said network nodes prior to said processing blocks commencing said processing functions.

3(Original). The circuit of Claim 1 further comprising a programming bus for transmitting said connection information to each of said network nodes.

4(Original). The circuit of Claim 1 wherein each of said buses is a serial bus.

5(Original). The circuit of Claim 1 wherein said two dimensional array comprises a rectangular array in which said network nodes are organized as a plurality of rows and columns.

6(Currently Amended). ~~The circuit of Claim 1~~ A circuit comprising:

a plurality of processing blocks on a first substrate; and

an interconnect network comprising a plurality of network nodes arranged in a two-dimensional array on said first substrate, each network node having a plurality of adjacent network nodes and being connected to each adjacent network node by a communication bus that connects only those two network nodes and processing blocks adjacent to that bus;

each network node comprising:

a plurality of communication ports, each communication port comprising an input port for receiving digital signals and an output port for transmitting digital signals on a bus connected to that communication port;

a programmable switch that selectively connects one of said input ports to one of said output ports in response to connection information stored in a memory in that network node, wherein:

each processing block is connected to one of said communication buses and sends and/or receives data on that bus, each processing block performing a predetermined processing function, said processing block being located within said two-dimensional array of network nodes, said circuit further comprising:

a second substrate that overlies said first substrate, said second substrate comprising an interconnect network comprising a plurality of network nodes arranged in a two-dimensional array on said second substrate, each network node having a plurality of adjacent network nodes and being connected to each adjacent network node by a communication bus that connects only those two network nodes;

each network node comprising:

a plurality of communication ports, each communication port comprising an input port for receiving digital signals and an output port for transmitting digital signals on a bus connected to that communication port;

a programmable switch that selectively connects one of said input ports to one of said output ports in response to connection information stored in a memory in that network node,

wherein at least one of said network nodes on said second substrate is connected to a corresponding network node on said first substrate by a bus that connects only those two network nodes.

7(Original). The circuit of Claim 1 wherein one of said processing blocks specifies said connection information that is stored in each of said network nodes.

8(Original). The circuit of Claim 7 wherein said one of said processing blocks also comprises an interface for receiving said connection information from a source external to said circuit.

9(Currently Amended). ~~The circuit of Claim 1~~ A circuit comprising:

a plurality of processing blocks on a first substrate; and

an interconnect network comprising a plurality of network nodes arranged in a two-dimensional array on said first substrate, each network node having a plurality of adjacent network nodes and being connected to each adjacent network node by a communication bus that connects only those two network nodes and processing blocks adjacent to that bus;

each network node comprising:

a plurality of communication ports, each communication port comprising an input port for receiving digital signals and an output port for transmitting digital signals on a bus connected to that communication port;

a programmable switch that selectively connects one of said input ports to one of said output ports in response to connection information stored in a memory in that network node, wherein;

each processing block is connected to one of said communication buses and sends and/or receives data on that bus, each processing block performing a predetermined processing function, said processing block being located within said two-dimensional array of network nodes, said circuit wherein one of said processing blocks is a spare processing block that is capable of performing processing functions that are normally performed by a second one of said processing blocks if said second one of said processing blocks is defective.